Monolithic Power Systems

MP1018

Flat Panel Monitor CCFL Driver Controller

General Description

The MP1018 is a Cold Cathode Florescent Lamp (CCFL) driver controller optimized for flat panel monitor applications. Designed to run off 12 or 15V input supplies, the MP1018 can drive up to 30 lamps (150W) via four (4) external N Channel MOSFETs. Its full bridge architecture converts unregulated DC input voltages to the nearly pure sine waves required to ignite and operate CCF Lamps.

The MP1018 supports analog and burst dimming without the use of external components. It has soft on and off burst waveform shaping, lamp current regulation, transformer secondary current regulation, output over voltage protection and a dual mode fault timer.

The MP1018 is available in the 28 lead TSSOP and SOIC packages.

Features

- Drives 4 External, Low Cost, N Channel FETs
- Drives up to 30 Lamps (150W)
- Operates with 12V or 15V Input Supplies
- Lamp Current and Voltage Regulation
- Analog and Burst Mode Dimming Control
- Integrated Burst Mode Oscillator and Modulator
- Burst Mode, Soft On and Soft Off
- Open/Short Lamp Protection
- Output Short Circuit Protection
- Automatic Recovery From ESD Event
- **Evaluation Board Available**

Applications

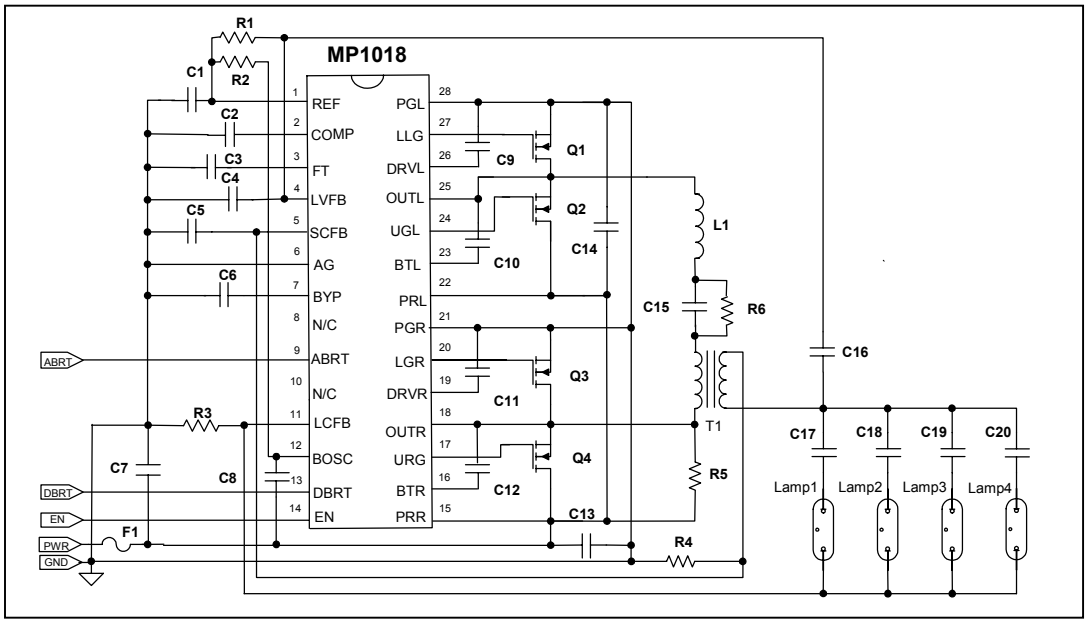
- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays
- LCD TVs and Monitors

Ordering Information

Part Number*	Package	Temperature
MP1018EM	TSSOP28	-20 to +85°C
MP1018EY	SOIC28	-20 to +85°C
EV0019	MP1018 Evaluation Board	

* For Tape & Reel, use suffix –Z (MP1018EM-Z)

Figure 1: Typical Application Circuit



Absolute Maximum Ratings

Input Voltage $V_{PRR,}$ V_{PRL}	18.5V
Logic Inputs	-0.3V to 6.5V
Junction Temperature	150°C
Power Dissipation (**Note 1**)	1.2W
Junction Temperature	150°C
Lead Temperature (Solder)	260°C
Operating Frequency	150KHz
Storage Temperature	–55°C to +150 °C

Recommended Operating Conditions

Input Voltage $V_{PRR,}$ V_{PRL}	8V to 17.5V
Analog Brightness Voltage V_{ABRT}	0V to 1.9V
Digital Brightness Voltage V_{DBRT}	0V to 1.8V
Enable Voltage V_{EN}	0V to 5.0V
Operating Frequency	20KHz to 100KHz
Operating Frequency (Typical)	60KHz
Operating Temperature	-20°C to + 85°C

Thermal Characteristics

Thermal Resistance θ_{JA}	105°C/W

Electrical Specifications (Unless otherwise specified V_{PRR}=V_{PRL}=17.5V, T_A=25 °C)

Parameters	Symbol	Condition	Min	Typ	Max	Units
Reference Voltage						
Output Voltage	V_{REF}	I_{REF}=3mA	4.75	5.0	5.25	V
Reference Current	I_{REF}		3.0			mA
Line Regulation		8V < V_{PRR}=V_{PRL} < 17.5V			30	mV
Load Regulation		0 < I_{REF} < 3.0mA			30	mV
Supply Current (Note 1)						
Supply Current (disabled)		V_{EN}=0V			10	uA
Supply Current (enabled)		8V < V_{PRR}=V_{PRL} < 17.5V		1.6	2.5	mA
Shutdown Logic						
Fault Timer Threshold			1.1	1.2	1.3	V
Fault Timer Sink Current		V_{LVFB}=5V, V_{SCFB}=0V		1		µA
Fault Timer Source Current						
Open Lamp		V_{LVFB}=0.1V, V_{SCFB}=0V		1		µA
Secondary Overload		V_{SCFB}=1.4V		120		µA
Enable Input Voltage Low	$V_{(IL)\ EN}$				0.5	V
Enable Input Voltage High	$V_{(IH)\ EN}$		2.0			V
Output Drivers						
Gate Drive	V_G			6.3		V
Gate Pull-Down	R_{GD}	Note 2		0.5		Ω
Gate Pull-Up	R_{GU}	Note 2		6.0		Ω
Gate Pull-Up Current	I_{GU}	Note 2		250		mA
Current Limit Threshold	V_{IG}	Note 2		1.3		V
Ton(min)		V_{COMP}=0V, V_{PRR}=V_{PRL} =17.5V		500		ns
Ton(min)		V_{COMP}=0V, V_{PRR}=V_{PRL} =8V		1500		ns

Electrical Specifications (Continued) (Unless otherwise specified V_{PRR}=V_{PRL}=17.5V, T_A=25 °C)

Parameters	Symbol	Condition	Min	Typ	Max	Units
Brightness Control						
Sense full Brightness	$V_{(IL)}$	V_{ABRT}= 2.0V		800		mV
Sense full Dim	$V_{(IL)}$	V_{ABRT}= 0V		225		mV
Lamp Current regulation		8V < V_{PRR}=V_{PRL} < 17.5V		2	5	%
Burst Oscillator Sink Current	I_{BOSC}			380		μA
Burst Oscillator Peak Voltage	V_{BOSC}		1.7	1.8	1.9	V
Fault Loop Control						
Open Lamp Threshold	$V_{(TH)\ VLFB}$			0		V
Secondary Current Threshold	$V_{(TH)\ CSFB}$			1.2		V
Fault Mode Comp Current	I_{COMP}	V_{VLFB}<0V, V_{CSFB}>1.2V		450		μA

Note 1: The input current is the sum of the current into PRR and PRL.
Note 2: This parameter is guaranteed by design.

Pin Description

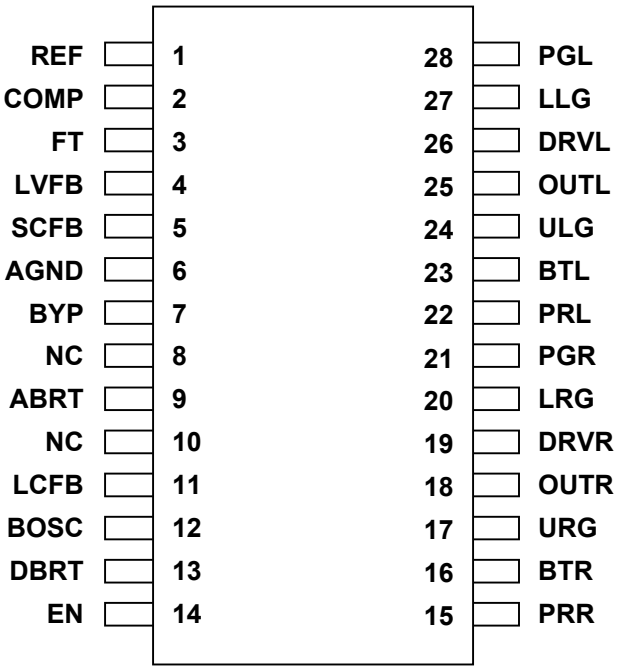
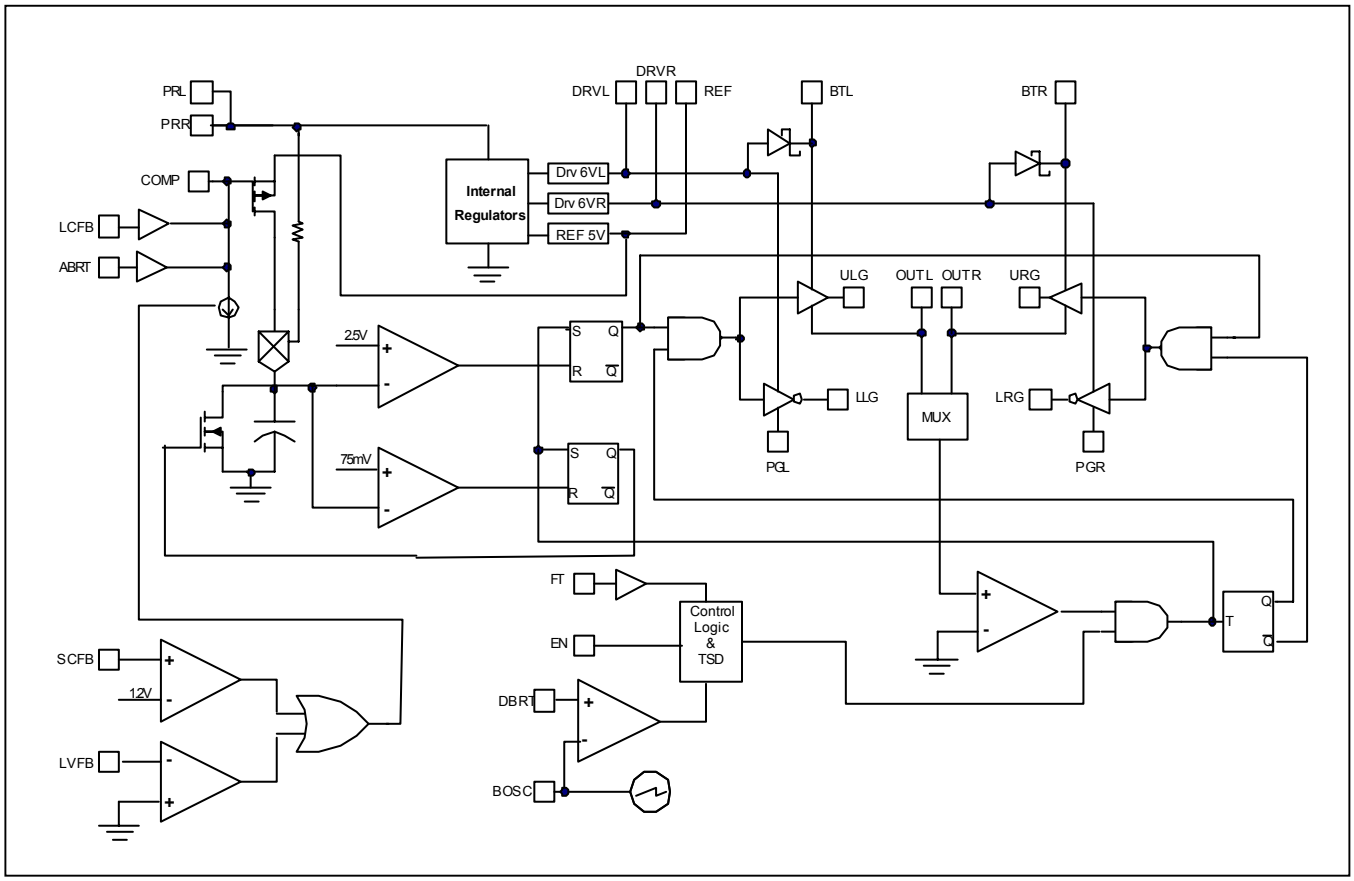


Table 1: Pin Designators

Pin No.	Pin Name	Pin Function
8,10	-------	Not Connected
1	REF	Internally Regulated 5V Reference Voltage. Bypass REF to AG with a 0.22µF or greater capacitor.
2	COMP	Regulation Loop Compensation Node. Connect a 2.2nF capacitor from COMP to AG to compensate the lamp current regulation loop.
3	FT	Fault Timing Capacitor. Connect a capacitor from FT to AG to set the fault timeout period.
4	LVFB	Lamp Voltage Regulation Feedback Input. Use a capacitor divider from the lamp to ground.
5	SCFB	Secondary Current Regulation Feedback Input. Connect a current sense resistor from the transformer secondary low-side to PGND to measure the secondary current.
6	AGND	Analog Ground
7	BYP	Bypass BYP to AG with a 1nF capacitor.
9	ABRT	Analog Brightness Control Input. Drive ABRT with a 0V to 2V DC voltage to adjust the brightness between fully dim and fully bright.
11	LCFB	Lamp Current Regulation Feedback Input. LCFB measures the lamp current through a resistor from the lamp low-side connection to ground.
12	BOSC	Burst-Mode Oscillator Timing. Place a capacitor from BOSC to GND and a resistor to REF to set the burst-mode frequency.
13	DBRT	Burst-Mode (Digital) Brightness Control Input. The voltage at DBRT controls the burst-mode duty cycle. The voltage ranges from 0V to 1.8V to set the duty cycle between Dmin to 100%
14	EN	Enable (On/Off) Input. Drive EN high to turn on the MP1018, drive it low to turn it off.
15	PRR	Input Power Rail, Right Side. PRR is the input power for the right-side MOSFET switches. Connect PRR to the input source at the drain of the right side high side MOSFET.
16	BTR	Bootstrap Capacitor, Right Side. BTR powers the right-side high-side MOSFET gate driver. Connect a 33nF capacitor from OUTR to BTR.
17	URG	High-Side MOSFET Gate Drive Output, Right Side. Connect URG to the gate of the right-side, high-side MOSFET.
18	OUTR	Bridge Power Output, Right Side. Connect the source of the right-side, high-side MOSFET, and the drain of the right-side, low-side MOSFET to OUTR.
19	DRVR	6V (Internally Generated) Drive Voltage Rail, Right Side. DRVR supplies power to the right-side MOSFET drivers URG and LRG. Bypass this pin with a 0.33µF capacitor.
20	LRG	Low-Side MOSFET Gate Drive Output, Right Side. Connect LRG to the right-side, low-side MOSFET gate. LRG swings between PGR and DRVR.
21	PGR	Power Ground, Right Side. Connect the source of the right-side MOSFET to PGR.
22	PRL	Input Power Rail, Left Side. PRL is the input power for the left-side MOSFET switches. Connect PRL to the input source at the drain of the left side high side MOSFET.
23	BTL	Bootstrap Capacitor, Left Side. BTR powers the left-side high-side MOSFET gate driver. Connect a 33nF capacitor from OUTL to BTL.
24	ULG	High-Side MOSFET Gate Drive Output, Left Side. Connect ULG to the gate of the left-side, high-side MOSFET.
25	OUTL	Bridge Power Output, Left Side. Connect the source of the left-side, high-side MOSFET, and the drain of the left-side, low-side MOSFET to OUTL.
26	DRVL	6V (Internally Generated) Drive Voltage Rail, Left Side. DRVL supplies power to the left-side MOSFET drivers ULG and LLG. Bypass this pin with a 0.33µF capacitor.
27	LLG	Low-Side MOSFET Gate Drive Output, Left Side. Connect LLG to the left-side, low-side MOSFET gate. LLG swings between PGL and DRVL.
28	PGL	Power Ground, Left Side. Connect the source of the left-side MOSFET to PGL.

Figure 2: Functional Block Diagram



Feature Description

Brightness Control

The MP1018 can operate in three modes: Analog Mode, Burst Mode with a DC input, or Burst Mode with an external PWM. The three modes are dependent on the pin connections as per Table 1. Choosing the required burst repetition frequency can be achieved by an RC combination, as defined in component selection. The MP1018 has a soft on and soft off feature to reduce noise, when using burst mode dimming. Analog dimming and Burst dimming are independent of each other and may be used together to obtain a wider dimming range.

Table 2: Function Mode

Function	Pin Connection		
	Pin 9	Pin 13	Pin 12
	ABrt	DBrt	Bosc
Analog Mode	0 – 1.9V	V_{Ref}	AGnd
Burst Mode with DC input voltage	V_{Ref}	0 – 1.8V	R2 C8
Burst Mode from external source	V_{Ref}	PWM	1.5V

Brightness Polarity:

Burst: 100% duty cycle is at 1.8V
Analog: 1.9V is maximum brightness

Feature Description (continued)

Fault Protection

Open Lamp: The LVFB pin (#4) is used to detect whether an open lamp condition has occurred. During normal operation the VLFB pin is typically at 5V DC with an AC swing of +/- 2V. If an open lamp condition exists then the AC voltage on the VLFB line will swing below zero volts. When that occurs, the IC regulates the voltage to 10V p-p and a 1µA current source will inject into the FT pin. If the voltage at the FT pin exceeds 1.2V, then the chip will shut down.

Excessive Secondary Current (Shorted Lamp): The SCFB pin (#5) is used to detect whether excessive secondary current has occurred. During normal operation the CSFB voltage is a 1V p-p AC signal centered at zero volts D.C. If a fault condition occurs that increases the secondary current, then the voltage at CSFB will be greater than 1.2V. When that occurs, the IC regulates the CSFB voltage to 2.4V p-p and a 120µA current source will inject into the FT pin. If the voltage at the FT pin exceeds 1.2V, then the chip will shut down.

Fault Timer: The timing for the fault timer will depend on the sourcing current, as described above, and the capacitor on the FT pin. The user can program the time for the voltage to rise before the chip detects a “real“ fault. When a fault is triggered, then the internal drive voltage (V_{Drv}) will collapse from 6.2V to 0V. The reference voltage will stay high at 5.0V. If no fault is detected a 1µA current sink will restore FT to 0V.

Lamp Startup

The strike voltage of the lamp will always be guaranteed at any temperature because the MP1018 uses a resonant topology for switching the outputs. The device will continue to switch at the resonant frequency of the tank until the strike voltage is achieved. This eliminates the need for external ramp timing circuits to ensure startup.

Chip Enable

The chip has an on / off function, which is controlled by the EN pin (#14). The enable signal goes directly to a Schmitt trigger. The chip will turn ON with an En = High and OFF with an En = Low.

Application Information

Pin 5 (SCFB) : R4, C5
(Secondary Short Protection)

The R4 and C5 combination is used for feedback to the SCFB pin to detect excessive secondary current. *These components should have +/- 5% tolerance limits.* The value for R4 is approximately 1KΩ and C5 is approximately 330nF. This will ensure that the voltage at the CSFB pin is typically 1.0V during steady state operation.

Pin 4 (VLFB): C16, C4 and R1
(Open Lamp protection)

The regulated open lamp voltage is proportional to the C16 and C4 ratio. C16 has to be rated at 3KV and is typically between 5 to 22pF. The value of C16 is typically 15pF and is chosen for a specified maximum frequency. The value of C4 is set by the customer to achieve the required open lamp voltage detection value, typically 4nF.

$$C4=C16 * V(max)rms/ 3.5Vrms)$$

The value of R1 is typically 300KΩ (not critical).

Pin 3 (FT): C3

The C3 cap is used to set the fault timer. This capacitor will determine when the chip will reach the fault threshold value. The user can choose the cap value to set the time out value.

Open Lamp Time

$$C3\ (nF) = T(open\ lamp)\ (1\mu A)/\ 1.2\ V$$

For a C3= 820nF, then the time out for open lamp will be 0.98 sec.

Secondary Short Turn Off time

Because the sourcing current for a secondary short is approx. 120µA, then the off time when a resistive short occurs across the lamp will be approx 100 times faster than the open lamp time.

Application Information (Continued)

To reduce the turn off time even further, then by modifying the connection at the FT node to:

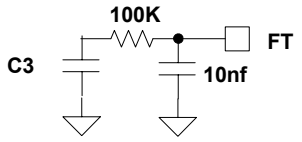


Figure 3: Turn Off Time Adjustment

For a Cap=10nF, then the time out for secondary short will be 0.11ms. The turn off time for the secondary short will be reduced by an additional 100 times.

Note: The open lamp time will remain the same value as defined by C3.

Pin 2 (COMP): C2

This cap is the system compensation cap that connects between COMP and AGnd. A 1.5nf or 2.2nF cap is recommended. This cap should be X7R ceramic with a voltage rating sufficient for 5V biasing. The value of C2 affects the soft-on rise time and soft-off fall time.

Pin 15 (REF): C1

C1 is the bypass cap for the internal 5.0V supply. This capacitor must be placed as close as possible to the pin. A maximum of 100 mils is recommended between the cap and the IC. The value of the cap is typically 0.47µF

Pin 15 (PRR), Pin 18 (PGR), Pin 21 (PGR), Pin 22 (PRL), Pin 25 (OUTL), Pin 28 (PGL)

These pins are used to sense the voltages across the external power transistors. These voltages are used by the MP1018 to protect the power transistors in the event of an accidental short from the output of the bridge to ground or the positive rail. It also detects the zero crossings of the AC current in the primary of the power transformer. A secondary function of the PRR and PRL (Positive Rail Right and Left) is to power the internal bias regulators (REF, DRVR and DRVL). PRR and PRL should make a Kelvin connection to the drains of the upper power transistors in the output bridge. PGR and PGL should make a Kelvin connection to the sources of the lower transistors in the output bridge. OUTR and OUTL should make a Kelvin connection to the sources of the upper transistors and the drains of the lower transistors in the output bridge.

Pin 13 (OUTL) & Pin 8 (OUTR): C15, R6, R5

The primary transformer current flows through this capacitor. Its value is typically 1µF and its voltage rating is sufficient for a 5V bias. The capacitor should be ceramic and have a ripple current rating greater than the primary current (typically 2Arms). It is more optimal to use two parallel 1µF ceramic caps for minimal ESR losses. R6 and R5 are used to ensure that the bridge outputs are at 0V prior to startup. Typically R5 = 2.7KΩ and R6 = 470Ω.

Pin 11 (BTL) and Pin 10 (BTR): C10 and C12

These are the reservoir caps for the upper switches' gate drive. They should be 10nF and made of X7R ceramic material and have a voltage rating for 6.6V biasing.

Pin 6 (DRV): C9

This bypasses the 6.2V gate supply for the lower switches. The value should be 100nF ceramic Y5V or X7R material.

Pin 5: (EN)

This pin will enable and disable the chip. Do not float this pin.

Pin 13 (DBRT)

This pin is used for burst brightness control. The DC voltage on this pin will control the burst percentage on the output. The signal is filtered for optimal operation. The active range is approximately 0.1V to 1.8V.

Pin 12 (BOSC): C8, R2

The C8 and R2 will set the burst repetition rate and the minimum burst time: $T_{MIN.}$ Set T_{MIN} to achieve the minimum required system brightness. Ensure that T_{MIN} is long enough that the lamp does not extinguish. These values are determined by the following steps:

Application Information (Continued)

1) Select a Minimum Duty Cycle, D_{MIN}, where:

$D_{MIN} = T_{MIN} * f_{BOSC}$

$D_{MIN} = T_{FALL} / (T_{FALL} + T_{RISE})$

2) Determine R2 by the formula:

$$R2 = \frac{\left[\frac{1.68 * [(1 / D_{MIN}) - 1]}{0.42}\right] + 4}{350 * 10^{-6}}$$

3) Select a burst frequency and then determine C8 by the formula:

$$C8 = \frac{(1-D_{MIN})}{0.42 * R2 * f_{bosc}}$$

Where:

f_{bosc}= burst frequency rate in Hz
T_{min}= Minimum burst time in sec

Figure 4: Burst Oscillator Waveform versus Output Lamp Current

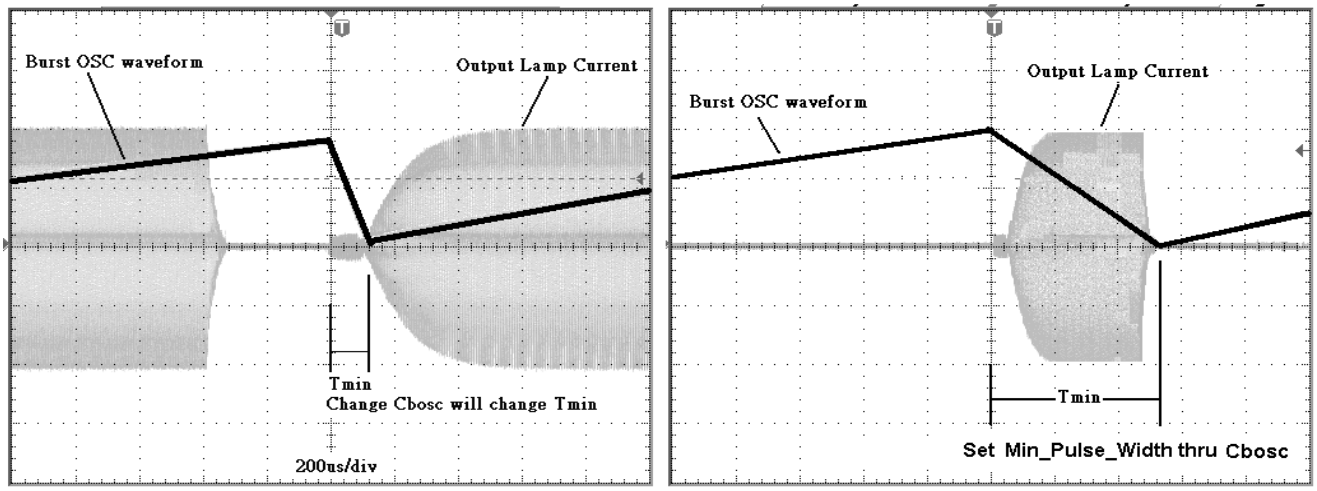
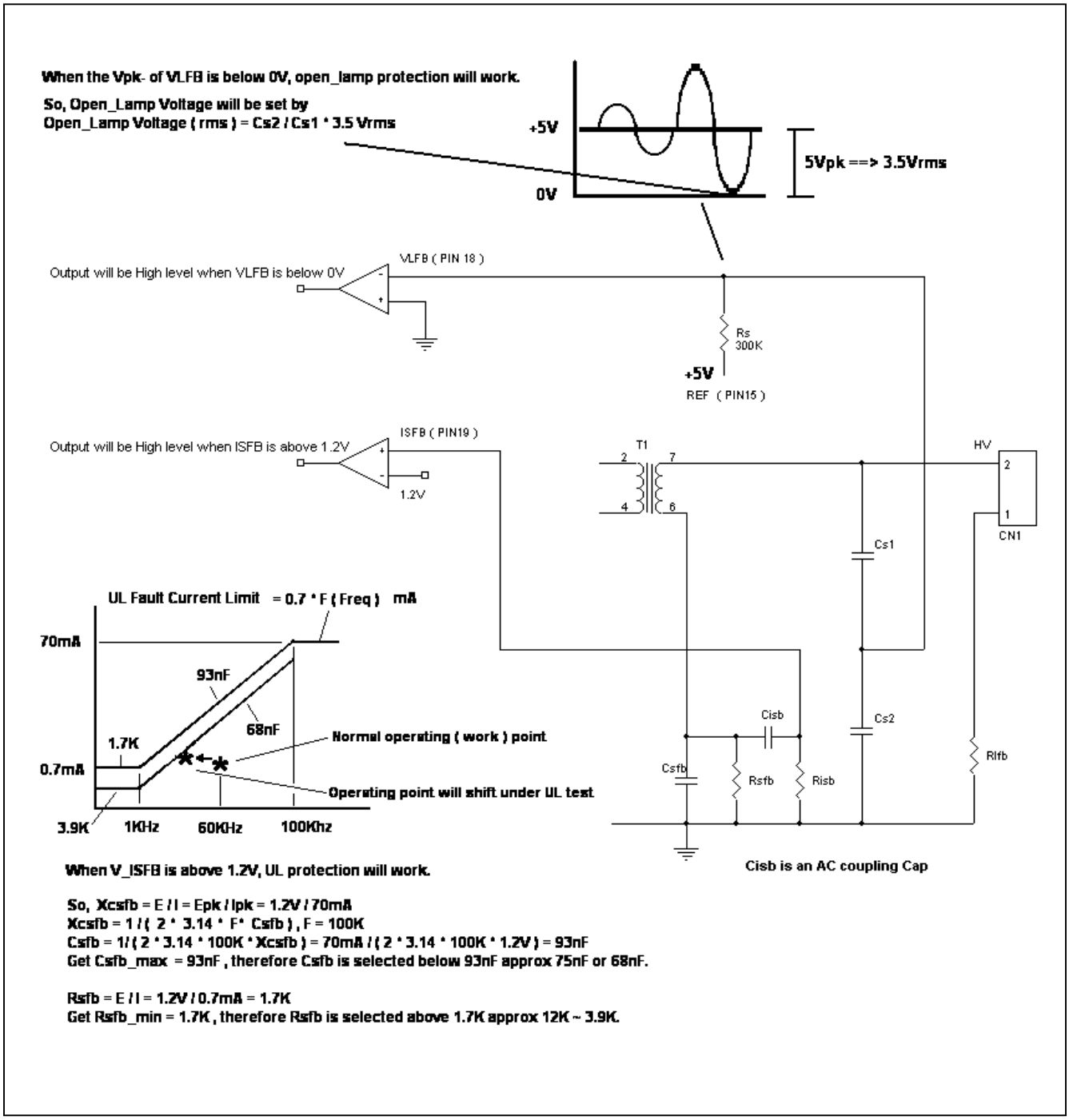
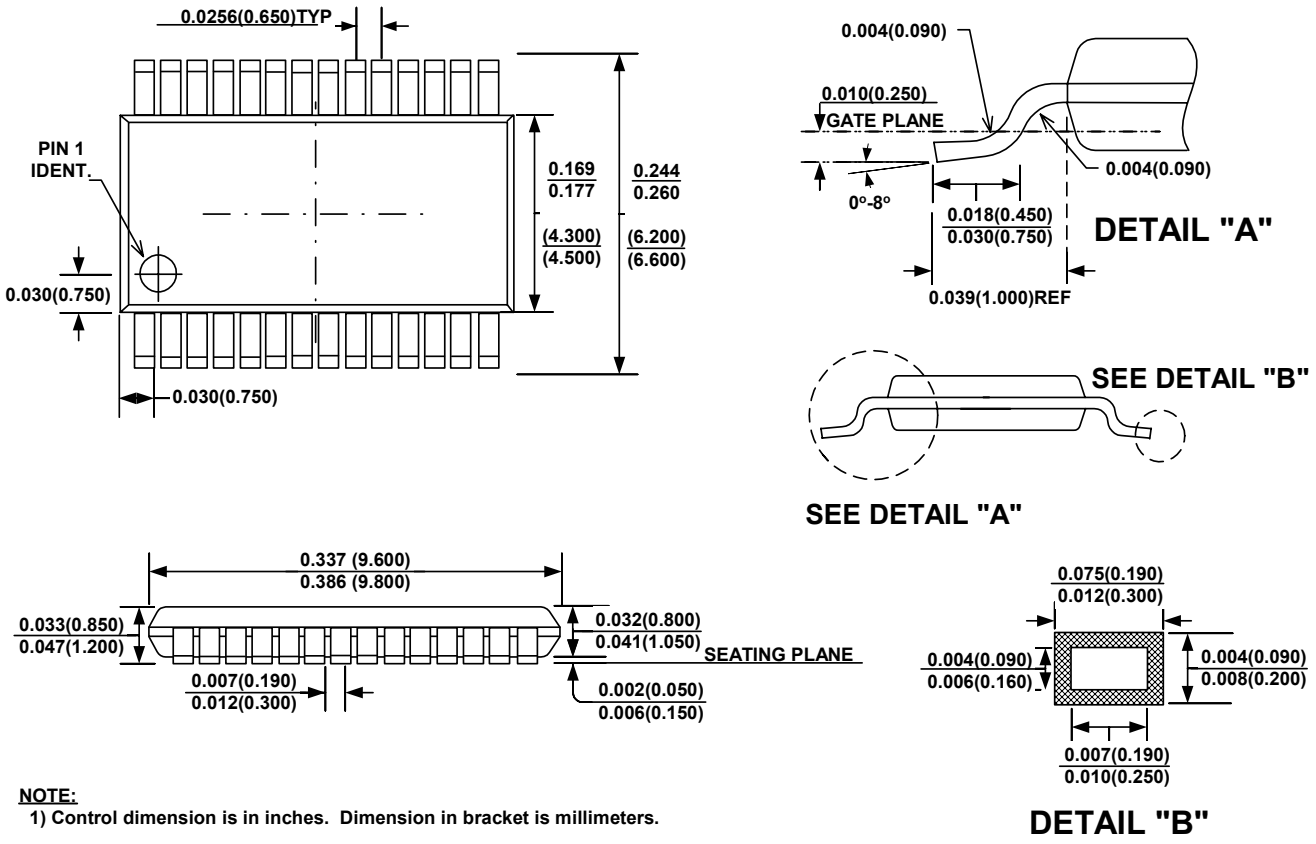


Figure 5: Open Lamp Voltage Setup and UL Test Protection Application Information



Package Information

TSSOP28



NOTE:
1) Control dimension is in inches. Dimension in bracket is millimeters.

Package Information

SOIC28